UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/884,175	06/19/2001	A. Kent Porterfield	303.760US1	2810

7590 08/31/2005

Schwegman, Lundberg, Woessner & Kluth, P. A.
Attn: Dana B. LeMoine
P.O. Box 2938
Minncapolis, MN 55402

EXAMINER	
TRAN, VINCENT HUY	
ART UNIT	**PAPER NUMBER**
2115	

DATE MAILED: 08/31/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/884,175	PORTERFIELD, A. KENT	
	Examiner	Art Unit	
	Vincent T. Tran	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-59* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24,26-30,32-47,49-52,54-56,58 and 59* is/are rejected.

7)☒ Claim(s) *25, 31, 48, 53, 57* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-59 are pending for examination.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claim 56 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. "indicate the existence of a capability".

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Rasmussen et al U.S. Patent 6,317,803 in view of Armstrong, II et al US 2002/0089318.

6. As per claim 1, Rasmussen et al teaches a apparatus comprising:

a hardware linked list [col. 40 lines 60-64], the hardware linked list including a plurality of nodes, each of the plurality of nodes including a next node pointer register [col. 41 lines 20-48].

Rasmussen et al further teach the capabilities pointer registers are set as read only. However, Rasmussen et al do not teach expressly the locking mechanism to conditionally make the next node pointer register of each of the plurality of nodes read-only.

Armstrong, II et al teach a register for reading and writing the operational information of a device. Specifically, Armstrong, II et al teach a locking mechanism to conditionally made the register read-only [paragraph 0020-0024].

Rasmussen et al and Armstrong, II et al are analogous art because they from the same field of endeavor – data accessing.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to have provided the system of Rasmussen et al with the locking mechanism of Armstrong, II et al to conditionally make the register read-only.

The motivation for doing so would have been to prevent unintentional or unauthorized write to the any register that hold important information, which could compromise the integrity of the system or device.

Therefore, it would have been obvious to combine the system of Rasmussen et al with Armstrong, II et al to obtain the invention as specified in claim 1.

7. Claims 1-7, 9-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rasmussen et al U.S. Patent 6,317,803 in view of Hall et al U.S. Patent 6,128,757.

As per claim 1, Rasmussen et al teaches a apparatus comprising:

a hardware linked list [col. 40 lines 60-64], the hardware linked list including a plurality of nodes, each of the plurality of nodes including a next node pointer register [col. 41 lines 20-48].

Rasmussen et al further teach the capabilities pointer registers are set as read only. However, Rasmussen et al do not teach expressly the locking mechanism to conditionally make the next node pointer register of each of the plurality of nodes read-only.

Hall et al teach a mechanisms to enhance the testability in an integrated computer system by providing access to the internal nodes of the modules within the integrate system, wherein each module of the device includes configuration registers and memory unit which store set-up and run time information concerning the operation of the module. Specifically, Larsen et al teach a locking mechanism to conditionally made the register read-only [col. 8 lines 45-63].

Rasmussen et al and Hall et al are analogous art because they from the same field of endeavor – peripheral initialization and configuration].

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to have modify the system of Rasmussen et al with the locking mechanism of Hall et al to conditionally make the register read-only.

The motivation for doing so would have been to ensure the integrity of the data containing in the registers are protected against unintended writes when data is written to the device or when a new code segment is updated [col. 8 lines 42-53].

Therefore, it would have been obvious to combine the system of Rasmussen et al with the locking mechanism of Hall et al to obtain the invention as specified in claim 1.

8. As per claim 2, Hall et al teach the locking mechanism comprises a control register [col. 8 lines 6-9].

9. As per claim 3, Rasmussen et al teach each of the plurality of nodes includes a register operable to specify a capability of the apparatus [col. 40 lines 60-65].

10. As per claim 4, Rasmussen et al teach the apparatus comprises a PCI local bus compliant peripheral device [col. 40 lines 1-15].

11. As per claim 5, Rasmussen et al teach the apparatus comprises an integrated circuit having a microprocessor bus compatible interface [inherent].

12. As per claim 6, Hall et al teach a hardware implemented capabilities list capable of being modified by low-level software [col. 7 lines 34-51], and read [col. 7 lines 52-55]. Hall et al do not expressly teach read only to higher level software. However, it would have been obvious to one of the ordinary in the art that the reading method of Hall et al including the claim higher level software since the specific level of software does not effect the operation of Hall method.

13. As per claim 7, Rasmussen et al teach the capabilities structure of the device is implemented as a linked list of register and each register node contains a NEXT PTR filed contains a pointer to the next item in the list. Therefore, according to the implementation of a

Linked List Algorithm (well know), it would have been obvious to one of ordinary skill in the art that Rasmussen et al system included the hardware implemented capabilities list comprises a plurality of list nodes that include a writable next node pointer register.

14. As per claim 9, Rasmussen et al teach the hardware implemented capabilities list is read-only to operating system software [col. 40 lines 66-67] and Hall et al teach the capabilities list is writeable by basic input output software [col. 7 lines 34-38].

15. As per claim 10, Rasmussen et al teach the PCI local bus compliant device comprises an integrated circuit that includes the hardware implemented capabilities list [col. 40 lines 60-63].

16. Claim 11-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Riley et al US 2002/0073258 in view of Larsen et al U.S. Patent 6,154,819.

17. As per claim 11, Riley et al teach an integrated circuit comprising:

an address bus [paragraph 0285];

a data bus [paragraph 0285];

a control bus [paragraph 0630];

a series of linked list register [paragraph 0676-0677] coupled to the address, data, control busses [paragraph 0669-0670], a series of linked list registers arranged in a readable linked list and configured as read-only. However, Riley et al do not teach expressly the series of linked list registers are writeable and a control register operable to lock the writeable linked list and conditionally make the series of linked list register read-only.

Larsen et al teach an apparatus for protecting register block in a programmable read only memory device. Larsen et al further teach a serious of register [col. 2 lines 46-49] coupled to the address, data, and control busses [fig. 700]. Specifically, Larsen et al teach a series of register arranged in a writeable list [col. 2 lines 49-54; col. 3 lines 47-53] and a control register operable to lock the writeable series of register and conditionally make the series of registers read-only [abstract, col. 7 lines 33-54].

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to have modified the system of Riley et al with the writeable register and a control register operable to lock and conditionally make the series of register read-only as taught by Larsen et al to enable the reprogramming and protecting of the information data registers utilize in a variety of devices or peripherals.

The motivation for doing so would have been to ensure the integrity of a series of register by providing a protection mechanism to protect stored data when the register is modified through program or erase operation [col. 1 lines 56-59].

Therefore, it would have been obvious to combine the system of Riley et al with Larsen et al to obtain the invention as specified in claim 11.

18. As per claim 12, Riley et al teach the series of linked list register are arranged in groups [paragraph 0675 – set of register], each group forming a linked list node, each linked list node including one next pointer register [paragraph 0675].

19. As per claim 13, Riley et al teach a linked list node which including a next node pointer register. Larsen et al tech the control register is operable to make the register read-only [obvious - see discussion in claim 11].

20. As per claim 14, Larsen et al teach the control register is accessible by a first level of software and the series of linked list registers are accessible by a second level of software, wherein the first level of software is lower than the second level of software [col. 7 lines 46-54; col. 8 lines 53-59].

21. As per claim 15, Riley et al teach the integrated circuit comprises a PCI local bus compliant computer peripheral [paragraph 0159, 0668-0669].

22. Claims 16, 18-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Roth U.S. Patent 6,430,666 in view of Larsen et al.

23. As per claim 16, Roth teaches an integrated circuit comprising:

a plurality of linked lists formed from register [14, 16, 18 fig. 1];

a head pointer register to point to one of the plurality of linked lists [HEAD fig. 1];

However, Roth does not teach a control register to conditionally make the head pointer register read-only.

Larsen et al teach an apparatus for protecting register block in a programmable read only memory device. Specifically, Larsen et al teach a control register to conditionally make the registers read-only [abstract, col. 7 lines 33-54].

Roth and Larsen et al are analogous art because they from the same field of endeavor – List data implemented in hardware.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to have modified the system of Roth with the control register of Larsen et al to enable the protection of registers.

The motivation for doing so would have been to ensure the integrity of the register by providing a protection mechanism to protect stored data when the register is unintentionally modified through program or erase operation [col. 1 lines 56-59].

Therefore, it would have been obvious to combine the system of Roth with Larsen et al to obtain the invention as specified in claim 16.

24. As per claim 18, Roth teaches each of the plurality of linked lists is from linked list nodes, each linked list node includes a writeable next node pointer register [col. 8 lines 4-24; col. 6 lines 31-43].

25. As per claim 19, Larsen et al teach the control register conditionally makes the writable register read-only [abstract].

26. Claims 17, 20-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Roth and Larsen et al as applied to claim 16 above, and further in view of Datta et al U.S. Patent 6,594,756.

27. As per claim 17, 20, Larsen et al teach a control register to conditionally make the register read-only. However, Larsen et al do not teach the control register is a write-once register.

Datta et al teach another system for protecting a register after reset. Specifically, Datta et al teach a write-once register [col. 3 lines 54-60].

Larsen et al and Datta are analogous art because they from similar problem solving area; data protection in register.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to have modified the system of Roth and Larsen et al with the write-once register to prevent the subsequent write.

The suggestion/motivation for doing so would have been to prevent update or reprogram a register during the normal operation of a system.

Therefore, it would have been obvious to combine Roth and Larsen et al system with Datta et al to obtain the invention as specified in claim 17.

28. As per claim 21, Datta et al teach the register can be written only once between system resets [col. 3 lines 56-59].

29. Claims 22-24, 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rasmussen et al in view of Datta et al and Larsen et al.

30. As per claim 22, Rasmussen et al teach an integrated circuit comprising:

a first register [PCI status register – col. 41 lines 3] to signify whether a capabilities list is enabled[1];

a second register to point to a capabilities list [col. 41 lines 21-22];

However, Rasmussen et al do not teach a first and second register as a writable register and a write-once control register operable to make the first and second writeable register read-only.

Larsen et al teach an apparatus for protecting register block in a programmable read only memory device. Further Larsen et al teach the lock register specifying whether a register is to be placed in a lock state or an unlocked state [abstract]. Specifically, Larsen et al teach a control register to conditionally make the registers read-only or writable [abstract, col. 7 lines 33-54].

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to have modified the system of Rasmussen et al with a writable register and the control register of Larsen et al to enable the resetting and protection of both first and second registers.

The motivation for doing so would have been to ensure the integrity of the register by providing a protection mechanism to protect the register setting when the register is unintentionally modified through program operation [col. 1 lines 56-59].

Larsen et al do not each the control register is a write-once register. Datta et al teach a write-once register [see discussion in claim 17].

Therefore, it would have been obvious to combine the system of Rasmussen et al with Larsen et al and Datta et al to obtain the invention as specified in claim 22.

---

[1] A bit in the PCI status register indicates the presence or absence of a capabilities list [table 4-1 – p. 41]

31. As per claim 23, Data et al teach the register can be written only once between system resets [see discussion in claim 21].

32. As per claim 24, Rasmussen et al teach a hardware linked list pointed to by the second writeable register [capabilities pointer register – col. 41 line 24], the hardware linked list including a plurality of nodes, each of the plurality of nodes comprising a writeable next node register [col. 41 lines 44-46].

33. As per claim 26, Rasmussen et al teach a PCI local bus compliant interface [abstract].

34. Claims 27-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Horan et al U.S. Patent 5,999,198 in view of Lin et al U.S. Patent 5,765,026 and Larsen et al.

35. As per claim 27, Horan et al teach an integrated circuit comprising:

a hardware linked list of register containing information for each capability supported by a peripheral device. Horan et al teach a group of register operable to indicate the capabilities of the integrated circuit. However, Horan et al do not teach expressly a plurality of register group.

Lin et al teach another method for creating a plurality of linked lists, wherein the method includes the step of retrieving a single selected portion of the combination of information form a linked list. Specifically, Lin et al teach a plurality of register groups, each register group including registers operable to indicate the state information of a system [col. 1 lines 43-48; col.

3 lines 22-27; col. 4 lines 12-27], and including a next group register to point to a next group [fig. 4].

Horan et al and Lin et al are analogous art because they from the same field of endeavor – Data management in memory.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to have modified the system of Horan et al with the plurality of linked list (group of register), each linked list including register operable to indicate the state information of the system as taught Lin et al to manage the different capabilities in a peripheral device.

The suggestion/motivation for doing so would have been to improve the access speed and reducing the storage requirement in a memory [col. 1 lines 29-32]; and

Larsen et al teach the control register operable to render the plurality of register groups read-only [see discussion in claim 16].

Therefore, it would have been obvious to combine Horan et al with Lin et al and Larsen et al to obtain the invention as specified in claim 27.

36. As per claim 28, Horan et al/Lin et al teach the plurality of register groups [Lin et al] form a PCI local bus compliant capabilities list [Horan et al –col. 17 lines 1-19].

37. As per claim 29, Larsen et al teach the control register cannot be modify through normal software command [col. 2 lines 62-65]. Therefore, it would have been obvious to one of ordinary skill in the art that the control register is modifiable once by basic input output software, and is not modifiable by operating system software.

38. As per claim 30, Larsen et al teach the control register comprises a write once lock bit, that when written, renders the plurality of register read-only [col. 8 lines 1-30].

39. Claims 32, 35-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Riley et al in view of Mitra et al U.S. Patent 6,167,472.

40. As per claim 32, Riley et al teach a computer system comprising:

a bus [109 fig. 1];

a memory device with basic input output software coupled to the bus [140 fig. 1];

a peripheral device couple to the bus [110, 122 fig. 1], the peripheral device including a capabilities list implemented in groups of registers [paragraph 0672-0677].

However, Riley et al do not teach a processor to execute instruction in the basic input output software to modify the capabilities list.

Mitra et al teach another method for allowing a host device to communicate with, and initialize, programs the peripheral device. Specifically, Mitra et al teach a processor to execute instruction in the basic input output software to modify the capabilities list [col. 2 lines 52-67; col. 3 lines 7-21; col. 4 lines 25-42].

Riley et al and Mitra et al are analogous art because they from the same field of endeavor – communicate and initializing an computer peripheral device],

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to have modified to system of Riley et al with the processor to execute instruction as taught by Mitra et al to modify the capabilities list

The suggestion/motivation for doing so would have been to enable the system to upgrade or modify the capabilities list of a peripheral device at any time since a typical PCI peripheral device configuration information cannot be changed once the configuration information is hard coded in the logic [col. 1 lines 37-49].

Therefore, it would have been obvious to combine the system of Riley et al with Mitra et al to obtain the invention as specified in claim 32.

41. As per claim 35, Mitra et al teach the peripheral device includes a PCI local bus compliant interface [col. 2 lines 48-49].

42. As per claim 36, Riley et al teach an add-in card upon which the peripheral device resides [fig. 1]

43. Claims 33-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Riley et al and Mitra et al as applied to claim 32 above, and further in view of Larsen et al.

44. As per claim 33, see discussion in claim 16.

45. As per claim 34, Mitra et al teach the memory device includes processor instructions stored therein to write to the register [col. 4 lines 43-59].

46. Claims 37-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mitra et al in view of Horan et al and Hall et al.

47. As per claim 37, Mitra et al teach a computer system comprising:

a PCI local bus compliant peripheral device coupled to a bus [114, 112 fig. 1]; and

a processor coupled to the bus [102 fig. 1];

wherein the PCI local bus compliant peripheral device includes a capabilities list modifiable by the processor [col. 4 lines 25-42].

However, Mitra et al do not teach expressly the capabilities list is a linked list and wherein the PCI local bus compliant peripheral device further includes a writeable control register operable to render the capabilities linked list read-only by the processor.

Horan et al teach a PCI local bus compliant peripheral device includes a capabilities list. Specifically, Horan et al teach the capabilities list is implemented as a linked list [col. 17 lines 16-20]. At the time of the invention was made, it would have been obvious to the person of ordinary skill in the art to have modified the capabilities list of Mitra et al with the linked list as taught by Horan et al in order to increase the access speed and to simplifying the modification process.

Hall et al teach writeable control register operable to render the capabilities register [col. 5 lines 28-12] read-only by processor [col. 5 line 45 to col. 6 line 6; col. 8 lines 42-53].

Mitra et al and Hall et al are analogous art because they from the same field of endeavor – peripheral initialization and configuration].

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to have modify the system of Mitra et al with the locking mechanism of Hall et al to conditionally make the register read-only.

The motivation for doing so would have been to ensure the integrity of the data containing in the registers are protected against unintended writes when data is written to the device or when a new code segment is updated [col. 8 lines 42-45].

Therefore, it would have been obvious to combine the system of Mitra et al and Horan et al with the locking mechanism of Hall et al to obtain the invention as specified in claim 37.

48. As per claim 38, Horan et al teach the capabilities linked list comprises a plurality of nodes make up of groups of registers, each node corresponding to one capability [col. 17 lines 15-19; col. 24 lines 44-50]. Hall et al teach the writeable register [col. 7 lines 34-38]. Therefore, At the time of the invention was make, it would have been obvious to one of ordinary skill in the art that the combine teachings of Horan et al and Hall et al included the claim the writeable next node pointer register.

49. As per claim 39, Hall et al teach the writeable control register is operable to render the writeable next node pointer register read-only [col. 8 lines 50-53].

50. As per claim 40, Mitra et al teach a memory device having processor instruction stored therein, the processor instruction being operable to cause the processor write to the writeable register [col. 4 lines 43-59]. Hall et al teach the access to the configuration registers is determined by the setting of the control register bit [col. 8 lines 50-53]. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that the combine

teachings of Mitra et al and Hall et al included the claim the teaching of the processor instructions being operable to cause the processor to write to the writeable control register.

51. As per claim 41, Horan et al teach the PCI local bus compliant peripheral device includes a register to indicate whether the capabilities linked list is enabled [PCI status register – see further explanation in claim 22]. Horan et al do not teach a writeable register. However, Mitra et al teach a programmable PCI peripheral device such that it would have been obvious to one of ordinary skill in the art that the combine teachings of Horan et al and Mitra et al included the claim the writeable register to indicate whether the capabilities linked list is enabled.

52. Claims 42-44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rasmussen et al in view of Lin et al and Hall et al.

53. As per claim 42, Rasmussen et al teach a hardware linked list [col. 40 line 61]comprising:

a list node having a capabilities register and a next node pointer register [col. 41 lines 21-46]. However, Rasmussen et al do not teach a control register or a second list node.

Hall et al teach a control register [see discussion in claim 1].

Lin et al teach another method for creating a plurality of linked lists, wherein the method includes the step of retrieving a single selected portion of the combination of information form a linked list. Specifically, Lin et al teach a first list node and a second list node [fig. 4].

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to have modified the system of Horan et al with the first list node and a second list node of Lin et al for indicating the capabilities of a peripheral device.

The suggestion/motivation for doing so would have been to simplify the process of modifying the capabilities list of a peripheral device [col. 1 lines 29-32]; and

Hall et al teach the register of the first and second list are conditionally read-only in response to the control register [see discussion in claim 1].

Therefore, it would have been obvious to combine Rasmussen et al with Lin et al and Hall et al to obtain the invention as specified in claim 27.

54. As per claim 43, Rasmussen et al teach a head pointer [capabilities pointer register – col. 41 lines 21-22] to point to the first list node and Hall et al teach a writeable register being conditionally read-only response to the control register [see discussion in claim 1]. Therefore, it would have been obvious to one of ordinary skill in the art that the combine teachings of Rasmussen et al and Hall et al included the claim the writeable head pointer register being conditionally read-only in response to the control register.

55. As per claim 44, Rasmussen et al teach the hardware linked list is compliant with a PCI local bus rev. 2.1 capabilities list [col. 41 table 4-1]. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was make that the Rasmussen et al system included the claim rev. 2.2.

56. Claims 45-46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rasmussen et al, Lin et al, and Hall et al as applied to claim 42 above, and further in view of Sibigtroth U.S. Patent 4,580,246.

57. As per claim 45, Lin et al do not teach expressly the control register is a write-once register. Sibigtroth teaches another write protection circuit for a control register which determined system configuration. Specifically, Sibigtroth teaches a control register is a write-once register [col. 1 lines 9-13]. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was make to have modified the control register of Hall et al with the write once register of Sibigtroth in order to provide the system the abilities to modify the setting of the peripheral device at a later time which were otherwise not available.

58. As per claim 46, Sibigtroth teaches the control register can be written to only once between hardware resets [col. 1 lines 10-13].

59. Claims 47, 49, 51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rasmussen et al in view of Mitra et al and Hall et al.

60. As per claim 47, Rasmussen et al teach a method of initializing a computer peripheral comprising:

reading a list of capabilities in a hardware linked list within the computer peripheral. However, Rasmussen et al do not teach expressly the writing a list of capabilities to node and writing to a control register within the computer peripheral to make the nodes read-only.

Mitra et al teach another system for allowing a host device to configured a peripheral device during the initializing a computer peripheral. Specifically, Mitra et al teach the writing of the capabilities list to a hardware register within the computer peripheral [col. 4 lines 25-33].

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to have modified to system of Rasmussen et al with the writing of the capabilities list to the hardware register as taught by Mitra et al to initializing a computer peripheral device.

The suggestion/motivation for doing so would have been to provide the system the abilities to reprogram or upgrade a peripheral device at a different time which otherwise was not possible for a hard coded logic system.

Hall et al teach the writing to a control register within to make the register read-only [see discussion in claim 1].

Therefore, it would have been obvious to combine Rasmussen et al with Mitra et al and Hall et al to obtain the invention as specified in claim 47.

61. As per claim 49, Hall et al teach the writing to a control register comprises writing once to a capabilities lock bit, which thereafter is read-only [col. 8 lines 50-53].

62. As per claim 51, It would have been obvious to one of ordinary skill in the art at the time of the invention that the performed by basic input output software was done prior to loading of an operating system. Since, during the loading of the operating system, the system required to initialize the peripheral device by detecting and providing resource for the peripheral according to its capabilities; therefore, the peripheral would be un-operative if the modification (performed basic input output software) after the operating system was load.

63. Claim 50 is rejected under 35 U.S.C. 103(a) as being unpatentable over Rasmussen/Mitra/Hall et al as applied to claim 47 above, and further in view of Sibigtroth.

64. As per claim 50. Rasmussen et al teach a capabilities list enabled register to signify whether the list of capabilities is enabled [see discussion in claim 22]. However, Rasmussen et al do not teach expressly the writing to the capabilities list enabled register. Sibigtroth teaches the writing to a control register [see discussion in claim 45]. Therefore, at the time of the invention was make, it would have been obvious to one of ordinary skill the art that the combine teachings of Rasmussen et al and Sibigtroth included the claim writing to a capabilities list enabled register.

65. Claim 52 is rejected under 35 U.S.C. 103(a) as being unpatentable over Rasmussen et al in view of Mitra et al and Hall et al.

66. As per claim 52, Rasmussen et a teach a method of initializing a PCI local bus compliant device comprising:

reading a list of capabilities in a hardware linked list within the computer peripheral. However, Rasmussen et al do not teach expressly reading instructions from a memory device holding basic input output software, modifying a link within a capabilities linked list and writing to a control register device to make the link read-only.

Mitra et al teach the reading instruction from a memory device holding basic input output software and modifying a link within a capabilities list [col. 4 lines 43-59 – see further discussion in claim 47]; and

Hall et al teach the writing to control register to make the register read-only [see discussion in claim 49]

Therefore, it would have been obvious to combine Rasmussen et al with Mitra et al and Hall et al to obtain the invention as specified in claim 52.

67. Claims 54-55 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rasmussen/Mitra/Hall et al as applied to claim 52 above, and further in view of Sibigtroth.

68. As per claim 54. see discussion in claim 50.

69. As per claim 55, Sibigtroth teaches the writing to writing to a control register, therefore, Sibigtroth teaches the claim writing to the head pointer register since the system would be un-operative if the system was not able to write to the head pointer register.

70. Claims 56, 58-59 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rasmussen et al in view of Mitra et al and Hall et al.

71. As per claim 56, Rasmussen et al teach the capabilities structure is implemented a linked list of register containing information for each function supported by the device and the PCI status register of the device indicates the presence or absence of a capabilities list. However, Rasmussen et al do not teach express the modifying a next node pointer register in a PCI local bus peripheral to indicate the existence of a capability and modify a control register in the PCI local bus peripheral to make the next node pointer register read-only.

Mitra et al Mitra et al teach another system for allowing a host device to configured a peripheral device during the initializing a computer peripheral. Specifically, Mitra et al teach the modifying of a register to indicate the existence of a capability [col. 3 lines 51-58; col. 4 lines 31-42].

Therefore, at the time of the invention was make, it would have been obvious to one of ordinary skill in the art to have modified the next pointer register of Rasmussen et al with the modification to indicate the existence of a capability as taught by Mitra et al in order to provide the system the abilities to re-program the capabilities linked list by modifying the next node pointer register; and

Hall et al teach the modifying a control register to make the nest node pointer register read-only [see discussion in claim 52].

Therefore, it would have been obvious to combine Rasmussen et al with Mitra et al and Hall et al to obtain the invention as specified in claim 56.

72. As per claim 58, Mitra et al teach the apparatus comprises a read-only memory [col. 4 line 54].

73. As per claim 59, Hall et al teach a control register to lock and unlock a register to protect the register from unintentional write. Therefore, at the time of the invention was make, it would have been obvious to one of ordinary skill in the art that the method Hall et al included the claimed modifying the capabilities list enabled register become read-only responsive to the control register.

Allowable Subject Matter

74. Claims 25, 31, 48, 53, 57 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vincent T. Tran whose telephone number is (571) 272-7210. The examiner can normally be reached on 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas c. Lee can be reached on (57 1)272-3667. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vincent Tran

THOMAS LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100